AMENDMENTS TO THE DRAWINGS

The drawings are objected to for failing to show every feature of the invention specified in the claims. In response to the rejection, Applicant has amended Fig. 1 to include a programmable routing matrix 129. Applicant also submits that no new matter is added by the amendment. Applicant submits a replacement drawing sheet.

REMARKS

In the Office Action mailed December 23, 2004, the specification is objected to for incorporating essential material by reference to a publication. In response to the objection, Applicant has amended the specification to include material from "The Programmable Logic Data Book 2000", Chapter 3, published by Xilinx, Inc., which was incorporated by reference in Paragraph [0014] of the specification. In particular, Applicant has added text in paragraph [0014] related to the programmable routing matrix. Support for the text can be found on pages 3-11 and 3-12 of "The Programmable Logic Data Book 2000." Applicant has also amended paragraph [0014] to indicate that configurable logic blocks provide functional elements for constructing logic. Support for the amendment can be found on page 3-7 of "The Programmable Logic Data Book 2000." Applicant submits that no new matter is added by the amendment to paragraph [0014].

The drawings are objected to for failing to show every feature of the invention specified in the claims. As set forth in the AMENDMENTS TO THE DRAWINGS section of this response, Applicant has amended Fig. 1 to include a programmable routing matrix. Applicant also submits that no new matter is added by the amendment.

Claims 1-6 and 10-13 were pending. Applicant cancels claims 15-22 without prejudice and reserves the right to pursue these claims in a divisional application. New claims 23-32 have been added.

Claims 1-2, 4-6 and 10 are rejected under 35 USC §102(b) as being anticipated by Akao et al. (US Patent 5,307,464, hereinafter "Akao"). Claims 1-6 and 10-13 are rejected under 35 USC §103(a) as being obvious over "The Programmable Logic Data Book 2000" in view of Akao. Finally, claims 3 and 11-13 are rejected under 35 USC §103(a) as being obvious over Akao or "The Programmable Logic Data Book 2000" in view of Applicant's admission in paragraphs [0015] and [0016].

I. US Patent 5,307,464 to Akao

Akao relates to a single chip microprocessor comprising a central processing

unit and a means for implementing its peripheral functions embedded in the same semiconductor package. Unlike a conventional microprocessor having a variety of dedicated on-chip hardware peripheral circuits, Akao discloses a method for implementing the peripheral functions of the microprocessor by employing a sub-processor. In particular, Akao addresses deficiencies of conventional single chip microprocessors, such as modifying operation specifications and functions of a microcomputer, by implementing peripheral functions through software running on a sub-processor. However, Akao fails to disclose or suggest the use of configurable blocks as set forth in the amended claims, and as will be described in more detail below, clearly teaches away from Applicant's claims as amended.

II. Clarification of Issues raised in the "Response to Arguments" Section

In order to fully respond to the current Office Action, Applicant addresses issues raised in the "Response to Arguments" section of the Office Action, before addressing new claim amendments and arguments supporting patentability of the claims. Applicant believes that it is necessary to clarify issues raised in the Response to Arguments section so that any new amendments and arguments can be fairly considered.

In response to the suggestion that the RAM and EPROM of Akao disclose "a configurable logic block having circuitry capable of implementing a plurality of logic functions," Applicant respectfully requests reconsideration. It has been suggested in this and previous Office Actions that the RAM and EPROM are field programmable, and therefore meet the definition of "configurable logic block." It is also suggested in the "Response to Arguments" section of this Office Action that is "unclear what applicant's definition of "configurable logic block" is if they are different from the known memory arrays that are programmable." Southgate (U.S. Patent 5,968,161) is cited to support the interpretation that RAM or EPROM comprise a "configurable logic block." In particular, it is suggested that col. 4, lines 23-29 of Southgate discloses that an EPROM is a configurable logic block. However, Applicant respectfully submits that col. 4, lines 23-29 discloses that a programmable logic device (PLD) "configured in accordance with the present invention" could be implemented with any type of PLD,

including a programmable memory circuit (such as an EPROM). Southgate discloses an FPGA having a configurable CPU and a second programmable section. Although the circuit disclosed in Southgate could be implemented with an EPROM, the disclosure in col. 4, lines 23-29 does not indicate that an EPROM is a "configurable logic block." Rather, the disclosure in col. 4, lines 23-29 of Southgate merely indicates that the invention of Southgate could be employed with a "programmable memory circuit."

Further, in response to the statement in the "Response to Arguments" section of the current Office Action that "Akao uses software to control the logic of the RAM by loading/configuring the appropriate peripheral functions as selected by the user into the memory of the sub-processor 5," Applicant respectfully submits that loading software into a sub-processor does not disclose employing "a configurable logic block having circuitry capable of implementing a plurality of logic functions" as claimed by Applicant. As disclosed in paragraph [0014] of the specification as amended, a configurable logic block provides functional elements for constructing logic. Further, Akao contrasts loading software stored in a memory into a sub-processor to implement peripheral functions with logic configurations using PLDs or PLAs. In particular, Akao indicates that:

> (i) the microprocessor 1 "is superior in that information for defining peripheral functions can be generated easily at a high speed due to the fact that peripheral functions implementable by the sub-processor 5 are defined by a microprogram" (Col. 32, lines 19-24);
>
> (ii) "while operation control signals can also be generated by a wired logic configuration utilizing PLDs, "the logic design for defining peripheral elements inevitably requires much time and, in addition, the increased number of gate stages also introduces time delays in the operation" (Col. 32, lines 27-30); and
>
> (iii) implementable peripheral functions defined by a microprogram enable "an easier and faster generation of information defining the peripheral functions than a wired logic configuration employing PLDS, PLAs or others" (Col. 34, lines 27-31).

Finally, to address the questions raised in the "Response to Arguments" section, Applicant is not stating that configuring a configuration logic block does not require software, or that configurable logic blocks are not changeable once they have been programmed. Rather, Applicant is stating that loading software to a sub-processor does not disclose employing a configurable logic block as claimed.

III. Claims 1-2, 4-6 and 10 as amended are not anticipated by Akao

In response to the rejection of claims 1-2, 4-6 and 10, Applicant has further amended independent claims 1 and 6 to more clearly distinguish over Akao. In particular, Applicant has amended independent claims 1 and 6 to indicate that a bus coupled between the processor core and the configurable peripheral device "connects said processor core and said configurable peripheral device without using a sub-processor." Applicant respectfully submits that the claims as amended clearly distinguish over Akao. Akao teaches the use of a sub-processor controlled by a microprocessor, and described above, teaches away from the use of configurable logic to implement peripheral functions. Applicant submits that dependent claims 2, 4, 5 and 10 are allowable for the same reason that the independent claims are believed allowable.

IV. Claims 1-6 and 10-13 as amended are not obvious in view of "The Programmable Logic Data Book 2000" and Akao.

In response to the rejection of claims 1-6 and 10-13 under 35 USC §103(a) as being obvious in view of "The Programmable Logic Data Book 2000" and Akao, Applicant further submits that one skilled in the art would not look to Akao to modify a device described in "The Programmable Logic Data Book 2000," and that any combination of "The Programmable Logic Data Book 2000" and Akao would not lead to Applicant's claims as amended. To establish a *prima facie* case of obviousness, there must be some suggestion or motivation to modify a reference or to combine reference teachings. The test for obviousness is based upon what the combined teachings of the references would have suggested to one of ordinary skill in the art. Where the teachings of two or more prior art references conflict, the Examiner must

weigh the power of each reference to suggest solutions to one of ordinary skill in the art, considering the degree to which one reference might accurately discredit another. *In re Young*, 927 F.2d 588, 18 USPQ2d 1089 (Fed. Cir. 1991). MPEP 2143. Also, a prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore and Associates, Inc. V. Garlock, Inc.*, 721 F.2d 1540 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984). MPEP 2141.03. While "The Programmable Data Book 2000" generally describes the use of configurable logic, Akao clearly teaches against using configurable logic for peripheral devices. Particularly, there is no teaching or suggestion in "The Programmable Logic Data Book 2000" to implement a configurable peripheral device comprising a configurable logic block. More importantly, the Akao reference clearly teaches away from implementing a configurable peripheral device in a configurable logic block. Finally, Applicant notes that the claims as amended clearly show a structural difference compared to the prior art. Accordingly, the combined teachings of the references would have suggested to one of ordinary skill in the art to employ a microprogram in a sub-processor to implement the peripheral functions.

Finally, Applicant further submits that claims 2-5 and 10-13, which are based upon independent claims 1 and 6, are also allowable over the cited references for the same reasons that the independent claims are believed allowable.

V. Claims 3 and 11-13 are not obvious Over Akao or "The Programmable Logic Data Book 2000" in view of Applicant's Admission.

In response to the rejection of claims 3 and 11-13 under 35 USC §103(a) as being obvious over Akao or "The Programmable Logic Data Book 2000" in view of Applicant's admission in paragraphs [0015] and [0016], Applicant's respectfully submit that claims 3 and 11-13 are also allowable for the same reasons that independent claims are believed allowable.

VI. New Claims

Applicant adds new claims 23-32, including independent claim 29. Applicant respectfully submits that the new claims are also allowable over Akao, and that no

new matter is introduced by the new claims.

VII. Conclusion

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the Applicant's attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

Kim Kanzaki, Ph.D.
Attorney for Applicant
Reg. No. 37,652

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on March 15, 2005.

Pat Slaback
Name *Signature*